



UTILITY PATENT APPLICATION TRANSMITTAL

Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.

35.C13765

First Named Inventor or Application Identifier

HIDEKAZU TAKAHASHI

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

☐ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification Total Pages

3. ☒ Drawing(s) (35 USC 113) Total Sheets

4. ☒ Oath or Declaration Total Pages

- a. ☐ Newly executed (original or copy)
b. ☒ Unexecuted for information purposes
c. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]

i. ☐ **DELETION OF INVENTOR(S)**
Signed Statement attached deleting inventor(s)
named in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference (useable if Box 4c is checked)
The entire disclosure of the prior application, from which a copy of the
oath or declaration is supplied under Box 4c, is considered as being
part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)

- a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure ☐ Copies of IDS
Statement (IDS)/PTO-1449 Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. ☐ Small Entity ☐ Statement filed in prior application
Statement(s) Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☐ Other: _____

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No. ____/____

18. CORRESPONDENCE ADDRESS

☒ Customer Number or Bar Code Label

05514
(Insert Customer No. or Attach bar code label here)

or ☐ Correspondence address below

NAME

Address

City

State

Zip Code

Country

Telephone

Fax



CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	12-20 =	0	X \$ 18.00 =	\$ -0-
	INDEPENDENT CLAIMS (37 cfr 1.16(b))	1-3 =	0	X \$ 78.00 =	\$ -0-
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			\$260.00 =	\$ -0-
				BASIC FEE (37 CFR 1.16(a))	\$760.00
	Total of above Calculations =				\$760.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				
	TOTAL =				\$760.00

19. Small entity status

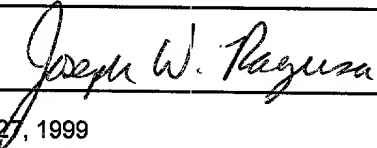
- a. ☐ A Small entity statement is enclosed
- b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
- c. ☐ Is no longer claimed.

20. ☒ A check in the amount of \$ 760.00 to cover the filing fee is enclosed.

21. ☐ A check in the amount of \$ _____ to cover the recordal fee is enclosed.

22. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:

- a. ☒ Fees required under 37 CFR 1.16.
- b. ☐ Fees required under 37 CFR 1.17.
- c. ☐ Fees required under 37 CFR 1.18.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	Joseph W. Ragusa (38,586)
SIGNATURE	
DATE	August 27, 1999

PHOTOELECTRIC CONVERTING APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to a photoelectric converting apparatus including a sensor unit and a memory unit.

Related Background Art

10 As one of conventional amplification type photoelectric converting apparatuses having sensor units, transfer units, and memory units, a CMOS inverting amplifier type sensor has been proposed in Japanese Patent Application Laid-open No. 09-200629, for example. The circuit arrangement of this

15 conventional sensor apparatus is shown in Fig. 1. In this drawing, reference numeral 1 denotes a PN photodiode for performing a photoelectric converting (transfer) operation; 2, an amplifying MOS transistor for constituting an inverting amplifier; 3, a switch

20 MOS transistor for supplying an output derived from a pixel to a vertical signal line 28; and 4, a resetting MOS transistor for resetting a potential of the photodiode. These circuit elements 1 to 4 constitute one pixel 5. Also, reference numeral 6 denotes a load

25 MOS transistor of the inverting amplifier, and this load MOS transistor 6 is provided every vertical line. Reference numeral 7 denotes a transfer gate used to

transfer pulses ϕ_{SL1} and ϕ_{PS1} which are employed to drive the respective pixels. The transfer gate 7 is controlled by a vertical scanning circuit 8. These circuit elements 1 to 8 constitute a sensor unit.

5 Also, reference numeral 9 denotes a switch MOS transistor for entering an output signal derived from a pixel of the sensor unit into a transfer unit; 10, a clamp capacitance; and 11, another switch MOS transistor for entering therein a clamp potential V_{GR} .

10 Reference numeral 12 denotes an amplifying MOS transistor of a source follower; 13, a constant current source of the source follower; 14, a switch MOS transistor for feeding back an output derived from a clamp circuit to a pixel of the sensor unit; 15, a switch MOS transistor for entering an output derived from a memory circuit to the clamp circuit; and 16, another switch MOS transistor for supplying an output signal derived from the clamp circuit to a memory pixel

21. These circuit elements 10 to 13 constitute the clamp circuit used to eliminate noise. Furthermore, the circuit elements 9 to 16 constitute the transfer unit. Also, reference numeral 17 denotes a memory capacitance; 18, an amplifying MOS transistor of the inverting amplifier; 19, a switch MOS transistor used to read an output signal derived from the memory pixel to the vertical signal line; and 20, another switch MOS transistor used to enter an output derived from a pixel

of the sensor unit, or from the transfer unit into the memory capacitance. These circuit elements 17 to 20 constitute a memory. Reference numeral 23 denotes a transfer gate for transferring memory drive pulses ϕ_{PS2} and ϕ_{SL2} , and this transfer gate 23 is driven by a vertical scanning circuit 24. Also, reference numeral 22 denotes a load MOS transistor of the inverting amplifier, and a single load MOS transistor 22 is provided every column. These circuit elements 17 to 24 constitute the memory unit.

Reference numeral 25 denotes a horizontal selection MOS switch. The horizontal selection MOS switch 25 is controlled by a horizontal scanning circuit 26 in such a manner that the output signals derived from the respective memory cells are outputted via an output amplifier 27 to an external circuit in a serial form.

In this conventional CMOS inverting amplifier type sensor, as to the pixel cell of the sensor unit and the memory of the memory unit, since the circuits for constituting the inverting amplifiers are completely identical to each other, these inverting amplifier circuits are designed by employing the same parameters (for example, L , W , C_{ox} of MOS transistor). However, the gain of the inverting amplifier for the pixels of the sensor unit is equal to that of the inverting amplifier for the memory of the memory unit

under such a condition that the circuits of the above-mentioned conventional sensor are not operated. As a result, this conventional sensor owns the below-mentioned drawbacks.

5 That is, in the case that the conventional sensor circuit is actually operated, since the gain of the signal outputted from the pixel of the sensor unit is different from that of the signal outputted from the memory of the memory unit, noise cannot be correctly
10 removed.

 It should be noted that a gain obtained under such a condition that the circuit is not operated will be referred to as a "DC gain", whereas another gain obtained under such a state that the circuit is
15 actually operated will be referred to as an "AC gain" in the below-mentioned description.

 Also, for example, when the conventional photoelectric converting apparatus is employed as an auto-focus (AF) sensor of a single-lens reflex camera,
20 there are other drawbacks that precision of an AGC (automatic gain control) circuit and also precision achieved under low brightness photographic condition would be deteriorated.

25 SUMMARY OF THE INVENTION

 An object of the present invention is to provide a photoelectric converting apparatus capable of correctly

removing noise.

To achieve the above-described object, according to one aspect of the present invention, there is provided a photoelectric converting apparatus

5 comprising: a sensor unit including a plurality of pixels each having at least photoelectric converting means and first amplifying means for amplifying a signal derived from the photoelectric converting means to output the amplified signal; and a memory unit

10 including a plurality of memories each having at least storing means for storing therein the signal derived from the sensor unit and second amplifying means for amplifying a signal derived from the storing means to output an amplified signal; wherein a gain of the first

15 amplifying means is made different from a gain of the second amplifying means.

Other objects and features of the present invention will become apparent from the following specification and the accompanying drawings.

20

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 schematically shows a circuit diagram of the conventional photoelectric converting apparatus;

Fig. 2 schematically represents a circuit diagram of a photoelectric converting apparatus according to a

25 first embodiment through a third embodiment of the present invention;

Fig. 3 indicates an operation timing chart for explaining operations of the photoelectric converting apparatus shown in Fig. 2; and

Fig. 4 is an explanatory diagram for
5 illustratively explaining the operations of the photoelectric converting apparatus shown in Fig. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2 is a drawing for representing a
10 photoelectric converting apparatus according to a first embodiment, which may best show a feature of the present invention. The photoelectric converting apparatus includes, as shown in Fig. 2, a sensor unit for converting light into an electric signal to output
15 the electric signal, a memory unit for storing thereinto the electric signal derived from the sensor unit, and a transfer unit for transferring a signal outputted from the sensor unit to the memory unit. In this drawing, reference numeral 1 denotes a PN
20 photodiode for performing a photoelectric converting (transfer) operation; 2, an amplifying MOS transistor for constituting an inverting amplifier; 3, a switch MOS transistor for supplying an output derived from a pixel to a vertical signal line 28; and 4, a resetting
25 MOS transistor for resetting a potential of the photodiode. These circuit elements 1 to 4 constitute one pixel 5. Also, reference numeral 6 denotes a load

MOS transistor of the inverting amplifier, and this load MOS transistor 6 is provided every vertical line. Reference numeral 7 denotes a transfer gate used to transfer pulses ϕ_{SL1} and ϕ_{PS1} which are employed to drive the respective pixels. The transfer gate 7 is controlled by a vertical scanning circuit 8. These circuit elements 1 to 8 constitute the sensor unit. Also, reference numeral 9 denotes a switch MOS transistor for entering an output signal derived from a pixel of the sensor unit into the transfer unit; 10, a clamp capacitance; and 11, another switch MOS transistor for entering therein a clamp potential V_{GR} . Reference numeral 12 denotes an amplifying MOS transistor of a source follower; 13, a constant current source of the source follower; 14, a switch MOS transistor for feeding back an output derived from a clamp circuit to a sensor cell; 15 shows a switch MOS transistor for entering an output derived from a memory circuit to the clamp circuit; and 16, another switch MOS transistor for supplying an output signal derived from the clamp circuit to a memory 21. These circuit elements 10 to 13 constitute the clamp circuit used to eliminate noise. Furthermore, the circuit elements 9 to 16 constitute the transfer unit. Also, reference numeral 17 denotes a memory capacitance; 18, an amplifying MOS transistor of the inverting amplifier; 19, a switch MOS transistor used to read signal derived

from the memory capacitance 17 to the vertical signal line; and 20, another switch MOS transistor used to enter an output derived from a pixel of the sensor unit, or from the clamp unit into the memory capacitance. These circuit elements 17 to 20 constitute the memory 21. Reference numeral 23 denotes a transfer gate for transferring memory drive pulses ϕ_{PS2} and ϕ_{SL2} , and this transfer gate 23 is driven by a vertical scanning circuit 24. Also, reference numeral 22 denotes a load MOS transistor of the inverting amplifier, and a single load MOS transistor 22 is provided every column. These circuit elements 17 to 24 constitute the memory unit. Reference numeral 25 denotes a horizontal selection MOS switch. The horizontal selection MOS switch 25 is controlled by a horizontal scanning circuit 26 in such a manner that the output signals derived from the respective memory cells are outputted via an output amplifier 27 to an external circuit in a serial form.

The photoelectric converting apparatus of the present embodiment is characterized in that a DC gain of an inverting amplifier of a pixel is made different from an AC gain of an inverting amplifier of a memory.

Hereinafter, a description will now be more specifically made of a method for differing the gain of the inverting amplifier according to this embodiment. That is, in the circuit shown in Fig. 2, assuming that

a stray capacitance between the vertical output line and the photodiode is C_{SS} , a capacitance of this photodiode is C_{PDS} , another stray capacitance between the vertical output line and the memory capacitance is C_{SM} , a capacitance of the memory capacitance is C_{PDM} , the AC gain of the inverting amplifier of the pixel employed in the sensor unit is G_{ACS} , the AC gain of the inverting amplifier of the memory employed in the memory unit is G_{ACM} , the DC gain of the inverting amplifier of the pixel employed in the sensor unit is G_{DCS} , and also the DC gain of the inverting amplifier of the memory employed in the memory unit is G_{DSM} .

The AC gain G_{ACS} of the pixel, and the AC gain G_{ACM} of the memory are given as follows:

$$G_{ACS} = (C_{PDS} + C_{SS}) / \{C_{PDS} + (1 + G_{DCS})C_{SS}\} \cdot G_{DCS} \quad (1)$$

$$G_{ACM} = (C_{PDM} + C_{SM}) / \{C_{PDM} + (1 + G_{DCM})C_{SM}\} \cdot G_{DCM} \quad (2)$$

As a consequence, in order to make the AC gain G_{ACS} of the inverting amplifier coincident with the AC gain G_{ACM} , both the DC gain G_{DCS} of the inverting amplifier and the DC gain G_{DCM} may be determined which may satisfy the below-mentioned formula (3):

$$\begin{aligned} (C_{PDS} + C_{SS}) / \{C_{PDS} + (1 + G_{DCS})C_{SS}\} \cdot G_{DCS} = \\ (C_{PDM} + C_{SM}) / \{C_{PDM} + (1 + G_{DCM})C_{SM}\} \cdot G_{DCM} \end{aligned} \quad (3)$$

The photoelectric converting apparatus of this first embodiment is characterized in that the size (dimension) of the amplifying MOS transistor 2 of the pixel employed in the sensor unit is made equal to the

size of the amplifying MOS transistor 18 of the memory
employed in the memory unit, whereas the size of the
load MOS transistor 6 of the pixel employed in the
sensor unit is made different from the size of the load
5 MOS transistor 22 of the memory employed in the memory
unit. More specifically, it is preferable to
manufacture both the amplifying MOS transistor 2 and
the amplifying MOS transistor 18 by the minimum rule of
the manufacturing process thereof in view of
10 sensitivity. Also, since the memory capacitance 17 is
larger than the capacitance of the photodiode 1,
lowering of the gain caused by the adverse influence
made by the stray capacitance is small. As a
consequence, a size relationship between the MOS
15 transistor 6 and the MOS transistor 22 may be set as
follows:

$$W_6 / L_6 < W_{22} / L_{22},$$

assuming that a gate width of the MOS transistor 6 is
 W_6 , a gate length of this MOS transistor 6 is L_6 , a gate
20 width of the MOS transistor 22 is W_{22} , and a gate length
of the MOS transistor 22 is L_{22} .

If the gate width W_6 is made equal to the gate
width W_{22} , then the gate lengths may be set as follows:

$$L_6 > L_{22}$$

25 Alternatively, if the gate length L_6 is made equal
to the gate length L_{22} , then the gate widths may be set
as follows:

$$W_6 < W_{22}$$

Next, a signal flow of the photoelectric
converting operation by the photoelectric converting
apparatus according to the first embodiment will now be
5 summarized with reference to a schematic diagram of
Fig. 4.

(1) First, noise N_s of the sensor unit is read out
from the sensor unit, and then, is transferred to a
transfer system.

10 (2) In the transfer system, noise N_T of the
transfer system is added, and noise $(N_s + N_T)$ is
inputted to the sensor unit.

(3) The noise N_s of the sensor unit is added to an
inverted output $-(N_s + N_T)$, and finally noise $-N_T$ is
15 outputted from the sensor unit. This noise $-N_T$ is sent
to the transfer system.

(4) In the transfer system, this noise $-N_T$ is
inverted into an inverted signal N_T , and then noise N_T
of the transfer system is added to this inverted signal
20 N_T to obtain noise $2N_T$ which is sent to the memory unit.

(5) The sensor unit is entered to a light signal
accumulation operation period (noise $N_s + N_T$ is left in
sensor unit). During this light signal accumulation
operation period, a signal corresponding to the signal
25 charge accumulated in the sensor unit is read out.
This output signal corresponds to $(-S_1 - N_T)$, and is
transferred to the transfer system.

(6) In the transfer system, noise N_T of the transfer system is added to the signal $(-S_1 - N_T)$ to obtain a signal $-S_1$. This signal is outputted as a signal during the light signal accumulation operation period.

(7) In the sensor unit, the light signal accumulation operation is furthermore carried out, and a signal corresponding to a signal charge accumulated after the accumulation operation period is accomplished is read out, and then this read signal is stored into the transfer system. This output signal is $(-S_2 - N_T)$.

(8) Noise N_M of the memory unit is added to the inverted signal $-2N_T$ derived from the memory unit to produce noise $(-2N_T + N_M)$. Then, this noise is read into the transfer system.

(9) In the transfer system, a subtraction process is carried out by subtracting the signal $(-S_2 - N_T)$ from the noise $(-2N_T + N_M)$, and the noise N_T of the transfer system is added to the subtraction result to obtain a signal $(S_2 + N_M)$ which is transferred to the memory unit.

(10) The noise N_M of the memory unit is added to the inverted signal $(-S_2 - N_M)$ derived from the memory unit to thereby output an addition result $(-S_2)$.

Referring now to Fig. 2 and Fig. 3, the above-described operations (1) to (10) of the photoelectric converting apparatus will be described more in detail.

First of all, while both a signal ϕ_{RS} and another signal ϕ_{PS1} are set as "H" levels, the sensor unit is reset.

Next, after the signal ϕ_{PS1} is set to an "L" level,
5 the signal ϕ_{GR} is set to an "H" level. At this time, signals ϕ_{FT1} and ϕ_{FT2} are maintained under "H" level states. As a result, an electrode provided on the side of the common output line of the capacitance 10 in the transfer system is set to the potential of V_{RS} , and
10 another electrode of the capacitance 10 is set to the potential of V_{GR} .

Furthermore, after the signal ϕ_{GR} is set to an "L" level and the signal ϕ_{RS} is set to an "L" level, while both the signal ϕ_{SL1} and the signal ϕ_{L1} are set to "H" levels,
15 the sensor noise output from the sensor unit after being reset is read to the common output line (at this time, sensor noise is read out as N_s). The foregoing operations correspond to the operations defined in the above item (1).

20 Since the potential at the common output line is varied by the sensor noise component N_s , the potential at the other electrode of the capacitance 10 set under stray condition is also varied by the sensor noise component N_s . In such a case that the signal ϕ_{FT1} is set
25 to an "L" level, both the signal ϕ_{SL1} and the signal ϕ_{L1} are set to "L" levels, the signal ϕ_{FB1} is set to an "H" level, and furthermore, the signal ϕ_{PS1} is set to an "H"

level, the sensor noise N_s is transferred from the transfer system to the sensor unit. At this time, since the noise N_T of the transfer system is additionally provided with this sensor noise N_s , finally
5 the noise of $(N_s + N_T)$ is inputted to the sensor unit (namely, sensor cell transfer operation of noise). The foregoing operations correspond to the operations defined in the above-explained item (2).

Next, while both the signal ϕ_{FT1} and the signal ϕ_{FB2}
10 are set to "H" levels, and furthermore the signal ϕ_{GR} , the signal ϕ_{SL1} and the signal ϕ_{LS} are set to "H" levels, the noise N_s of the sensor unit is added to the inverted output signal $-(N_s + N_T)$ to eventually output noise $-N_T$ from the sensor unit. This noise $-N_T$ is sent to the
15 transfer system. At this time, a potential at the electrode provided on the side of the common output line of the capacitance 10 employed in the transfer system is varied by the noise component $-N_T$. On the other hand, a potential at the other electrode of this
20 capacitance 10 is fixed to V_{GR} . In addition, while the signal ϕ_{GR} is set to an "L" level, the other electrode of the capacitance 10 is brought into a stray condition (namely, noise reading operation). These foregoing operations correspond to the operations defined in the
25 above-described item (3).

Next, while both the signal ϕ_{RS} and the signal ϕ_{PS2} are set to "H" levels, a potential at the electrode

provided on the side of the common output line of the capacitance 10 employed in the transfer system becomes V_{RS} , and is varied by the noise component N_T . As a result, a potential at the other electrode of the capacitance 10 is similarly varied by the noise component N_T , and the noise N_T is transferred from the transfer system to the memory unit. At this time, since the transfer system noise N_T of the transfer system is added to this transferred noise N_T , noise $2N_T$ is eventually entered into the memory unit (namely, memory transfer operation of noise). The foregoing operations corresponds to the operations defined in the above-explained item (4).

Subsequently, the sensor unit is entered into the light signal accumulation operation period, and then, this sensor unit reads signals corresponding to signal charges accumulated in the sensor unit during this light signal accumulation operation period in the below-mentioned manner.

That is, while the signal ϕ_{GR} is set to an "H" level (at this time, signal ϕ_{RS} is maintained at "H" level), a potential at the electrode provided on the side of the common output line of the capacitance 10 of the transfer system is set to V_{RS} and a potential at the other electrode of the capacitor 10 is set to V_{GR} . Furthermore, the signal ϕ_{GR} is set to an "L" level, a potential at the other electrode of the capacitor 10 is

set to a stray condition. Thereafter, when the signal ϕ_{SL1} and the signal ϕ_{LS} are set to "H" levels, the noise N_s of the sensor unit is added to the inverted output $-(S_1 + N_s + N_T)$, so that a signal $(-S_1 - N_T)$ is
5 eventually outputted from the sensor unit to be supplied to the transfer system. These foregoing operations correspond to the operations defined in the above-described item (5).

Since a potential at the electrode provided on the
10 side of the common output line of the capacitance 10 employed in the transfer system is varied by the signal component $(-S_1 - N_T)$, a potential at the other electrode of the capacitance 10 is also varied by the same potential component to become $V_{GR} + (-S_1 - N_T)$. In such
15 a case that a signal is transferred from the transfer system, since the noise N_T of the transfer system is added to this signal, a signal $-S_1$ is eventually outputted from the transfer system. The foregoing operations correspond to the operations defined in the
20 above-described item (6).

Next, the light signal accumulation operation is further carried out in the sensor unit. After this light signal accumulation operation period is completed, when the signals ϕ_{SL1} , ϕ_{LS} , ϕ_{GR} , and ϕ_{FT2} are
25 set to "H" levels, a potential at the other electrode of the capacitance 10 of the transfer system is fixed to V_{GR} , and the potential at the electrode provided on

the side of the common output line of the capacitance 10 is varied from V_{RS} by the signal component $(-S_2 - N_T)$. It should be noted that the signal $(-S_2 - N_T)$ is equal to such a signal produced by adding the noise N_S of the sensor unit to the inverted output $-(S_2 + N_S + N_T)$ derived from the sensor unit. The foregoing operations correspond to the operations defined in the above-described item (7).

Next, when the signals ϕ_{SL2} and ϕ_{LM} are set to "H" levels, while the noise N_M of the memory unit is added to the inverted signal $-2N_T$ derived from the memory unit, a signal $(-2N_T + N_M)$ is read out to the electrode provided on the side of the common output line of the capacitance 10 employed in the transfer system (at this time, the other electrode of capacitance 10 of the transfer system is brought into stray condition). The foregoing operations correspond to the operations defined in the above-described item (8).

As a result, since the potential variation of the electrode provided on the side of the common output line of the capacitance 10 becomes $-(-S_2 - N_T) + (-2N_T + N_M) = S_2 - N_T + N_M$, the potential variation of the other electrode of the capacitor 10 similarly becomes $(S_2 - N_T + N_M)$. When the signals ϕ_{FB2} and ϕ_{PS2} are set to "H" levels, a signal $(S_2 - N_T + N_M)$ is transferred from the transfer system to the memory unit. At this time, since the noise N_T of the transfer system is also

produced, a signal ($S_2 + N_M$) is eventually entered into the memory unit. These operations correspond to the operations defined in the above-described item (9).

Subsequently, while both signal ϕ_{SL2} and signal ϕ_{LM} are set to "H" levels, a signal is read out from the memory unit to be outputted. In this case, since the noise N_M of the memory unit is added to the inverted signal ($-S_2 - N_M$), a sensor signal $-S_2$ from which the noise component has been removed may be eventually outputted.

In this first embodiment, random noise which is mixed with the signal when the sensor is reset may also be transferred to the memory unit during the operation (4). Then, since this random noise of the sensor unit is removed during the operation (9), a finally produced signal $-S_2$ may have a high S/N, which does not contain such a sensor random noise.

As previously described, in accordance with this first embodiment, since the ratio of W(width)/L(length) of the load MOS transistors is changed, the DC gain of the inverting amplifier employed in the pixel of the sensor unit is varied from the DC gain of the inverting amplifier employed in the memory of the memory unit. As a consequence, the AC gain adversely influenced by the stray capacitance can be made as an ideal value. In other words, since the above-explained operations are carried out, both the FPN of the signal output from

the pixel of the sensor unit and the FPN of the signal output from the memory of the memory unit can be reduced.

Next, a description will now be made of a photoelectric converting apparatus according to a second embodiment of the present invention.

Also, in this second embodiment, in order to make the AC gain G_{ACS} of the inverting amplifier coincident with the AC gain G_{ACM} , both the DC gain G_{DCS} of the inverting amplifier and the DC gain G_{DCM} may be made different from each other, which may satisfy the above-mentioned formula (3). To this end, the size (dimension) of the load MOS transistor of the pixel employed in the sensor unit is made equal to the size of the load MOS transistor of the memory employed in the memory unit, whereas the size of the amplifying MOS transistor of the pixel employed in the sensor unit is made different from the size of the amplifying MOS transistor of the memory employed in the memory unit. In other words, a size relationship between the MOS transistor 2 and the MOS transistor 18 may be set as follows:

$$W_2 / L_2 < W_{18} / L_{18} \text{ (note: } W_6 / L_6 = W_{22} / L_{22} \text{)},$$

assuming that a gate width of the MOS transistor 2 is W_2 , a gate length of this MOS transistor 2 is L_2 , a gate width of the MOS transistor 18 is W_{18} , and a gate length of the MOS transistor 18 is L_{18} .

If the gate width W_2 is made equal to the gate width W_{18} , then the gate lengths may be set as follows:

$$L_2 > L_{18}$$

Alternatively, if the gate length L_2 is made equal
5 to the gate length L_{18} , then the gate widths may be set as follows:

$$W_2 < W_{18}$$

It should also be understood that the photoelectric converting apparatus according to this
10 second embodiment may be operated in a similar manner to that of the first embodiment.

Subsequently, a photoelectric converting apparatus according to a third embodiment of the present invention will now be described.

15 Similar to the above-explained first and second embodiments, in order to make the AC gain G_{ACS} of the inverting amplifier coincident with the AC gain G_{ACM} of the inverting amplifier, this embodiment is characterized in that a gate oxide layer thickness of a
20 MOS transistor that constitutes the inverting amplifier of the pixel of the sensor unit, and a gate oxide layer thickness of a MOS transistor that constitutes the inverting amplifier of the memory of the memory unit are varied, which may satisfy the above-mentioned
25 formula (3).

In general, a mutual conductance g_m of a MOS transistor is given as follows:

$$g_m \propto (W/L) \cdot C_{ox} = W \cdot \epsilon_s \cdot \epsilon_o / LT_{ox}$$

As a consequence, to realize the above-described featured condition, the below-mentioned relationship may be established:

5 $T_{ox6} > T_{ox22},$

where symbol T_{ox6} implies the gate oxide layer thickness of the MOS transistor 6, and symbol T_{ox22} indicates the gate oxide layer thickness of the MOS transistor 22.

Alternatively,

10 $T_{ox2} > T_{ox18},$

where symbol T_{ox2} implies the gate oxide layer thickness of the MOS transistor 2, and symbol T_{ox18} implies the gate oxide layer thickness of the MOS transistor 18.

It should also be noted that the photoelectric
15 converting apparatus according to the third embodiment may be operated in a similar manner to that of the first embodiment.

While the present invention has been described as the first to third embodiments in which the circuit
20 arrangements of the photoelectric converting apparatuses are manufactured by employing the MOS transistors, the present invention is not limited thereto. For example, the photoelectric converting apparatus equipped with the sensor unit, the transfer
25 unit, and the memory unit may be manufactured by employing any types of transistors other than these MOS transistors, for instance, bipolar transistors.

Although the inverting amplifier is constituted by the amplifying transistor and the load transistor, this inverting amplifier may be arranged by other circuit arrangements capable of obtaining inverted outputs.

5 As previously described, in accordance with the photoelectric converting apparatuses of the first to third embodiments, noise can be minimized.

Also, when this photoelectric converting apparatus is utilized in an AF (auto-focus) system of a camera,
10 since noise may be reduced, for instance, a low brightness limit value and a low contrast limit value may be increased. As a result, there is such a merit that the performance of the AF system may be furthermore improved.

15 Many widely different embodiment of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the
20 specification, except as defined in the appended claims.

WAHT IS CLAIMED IS:

1. A photoelectric converting apparatus
comprising:

5 a sensor unit including a plurality of pixels each
having at least photoelectric converting means and
first amplifying means for amplifying a signal derived
from said photoelectric converting means to output the
amplified signal; and

10 a memory unit including a plurality of memories
each having at least storing means for storing
thereinto the signal derived from said sensor unit and
second amplifying means for amplifying a signal derived
from said storing means to output an amplified signal
wherein

15 a gain of said first amplifying means is made
different from a gain of said second amplifying means.

2. A photoelectric converting apparatus according
to Claim 1, wherein said first amplifying means and
20 said second amplifying means are constituted by MOS
transistors.

3. A photoelectric converting apparatus according
to Claim 2, wherein said first amplifying means and
25 said ~~second~~ amplifying means are constituted by both
amplifying MOS transistors and load MOS transistors.

4. A photoelectric converting apparatus according to Claim 3, wherein a conductance of the load MOS transistor included in said first amplifying means is made different from a conductance of the load MOS transistor included in said second amplifying means.

5. A photoelectric converting apparatus according to Claim 4, wherein a gate length of the load MOS transistor included in said first amplifying means is made different from a gate length of the load MOS transistor included in said second amplifying means.

6. A photoelectric converting apparatus according to Claim 4, wherein a gate width of the load MOS transistor included in said first amplifying means is made different from a gate length of the load MOS transistor included in said second amplifying means.

7. A photoelectric converting apparatus according to Claim 4, wherein a gate oxide layer thickness of the load MOS transistor included in said first amplifying means is made different from a gate oxide layer thickness of the load MOS transistor included in said second amplifying means.

8. A photoelectric converting apparatus according to Claim 3, wherein a conductance of the amplifying MOS

transistor included in said first amplifying means is made different from a conductance of the amplifying MOS transistor included in said second amplifying means.

5 9. A photoelectric converting apparatus according to Claim 8, wherein a gate length of the amplifying MOS transistor included in said first amplifying means is made different from a gate length of the amplifying MOS transistor included in said
10 second amplifying means.

 10. A photoelectric converting apparatus according to Claim 8, wherein a gate width of the amplifying MOS transistor included in said first
15 amplifying means is made different from a gate width of the amplifying MOS transistor included in said second amplifying means.

 11. A photoelectric converting apparatus
20 according to Claim 8, wherein a gate oxide layer thickness of the amplifying MOS transistor included in said first amplifying means is made different from a gate oxide layer thickness of the amplifying MOS transistor included in said second amplifying means.

25

 12. A photoelectric converting apparatus according to Claim 1, further comprising transferring

means for amplifying the signal derived from said sensor unit and/or said memory unit to transfer the amplified signal to said sensor unit and/or said memory unit.

ABSTRACT OF THE DISCLOSURE

In a photoelectric converting apparatus including a sensor unit, a transfer unit, and a memory unit, noise can be minimized. The photoelectric converting apparatus comprises a sensor unit including a plurality of pixels each having at least photoelectric converting means and first amplifying means for amplifying a signal derived from the photoelectric converting means to output the amplified signal, and a memory unit including a plurality of memories each having at least storing means for storing therein the signal derived from the sensor unit and second amplifying means for amplifying a signal derived from the storing means to output an amplified signal. Then, a gain of the first amplifying means is made different from a gain of the second amplifying means.

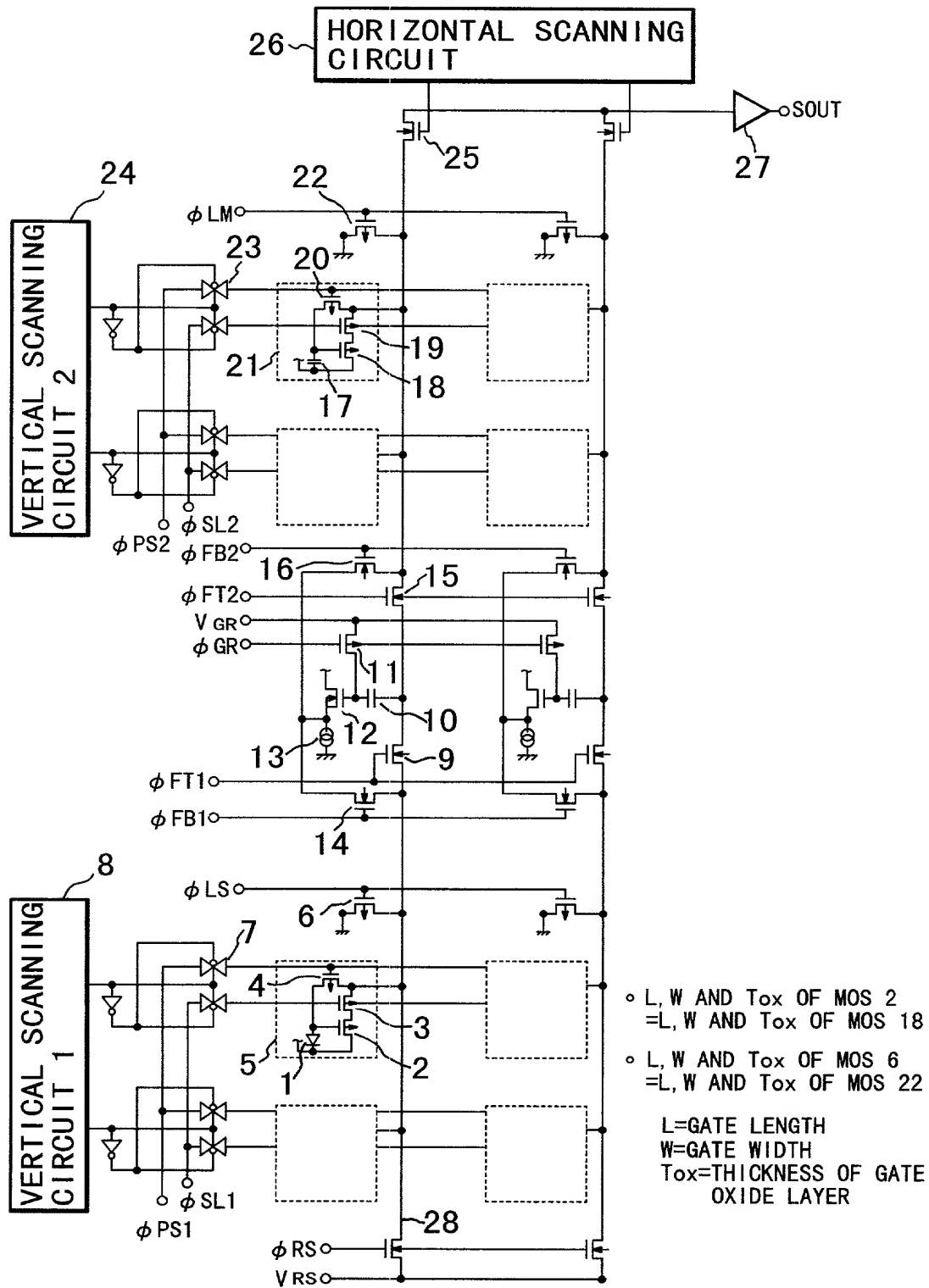


FIG. 1

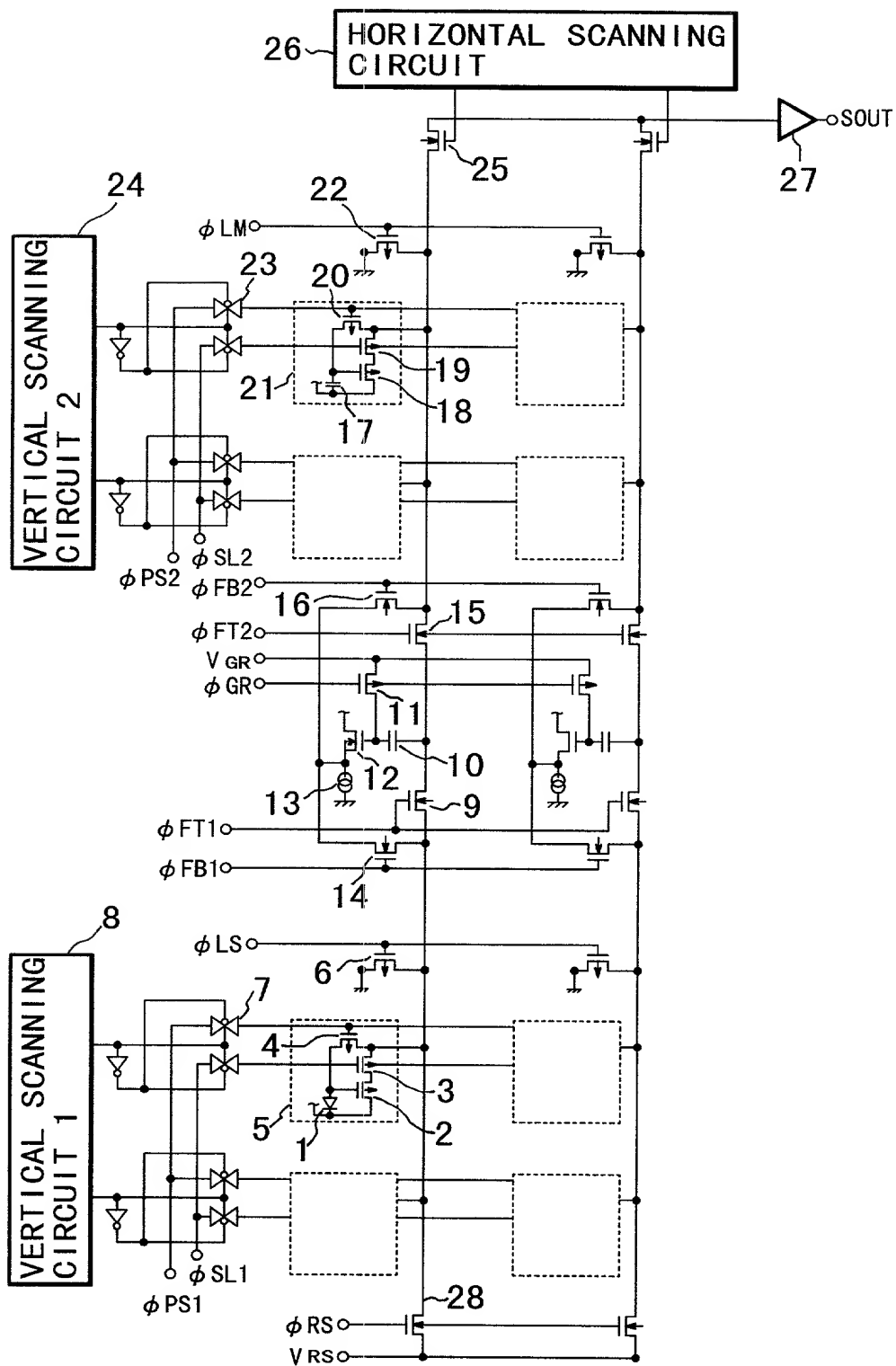


FIG. 2

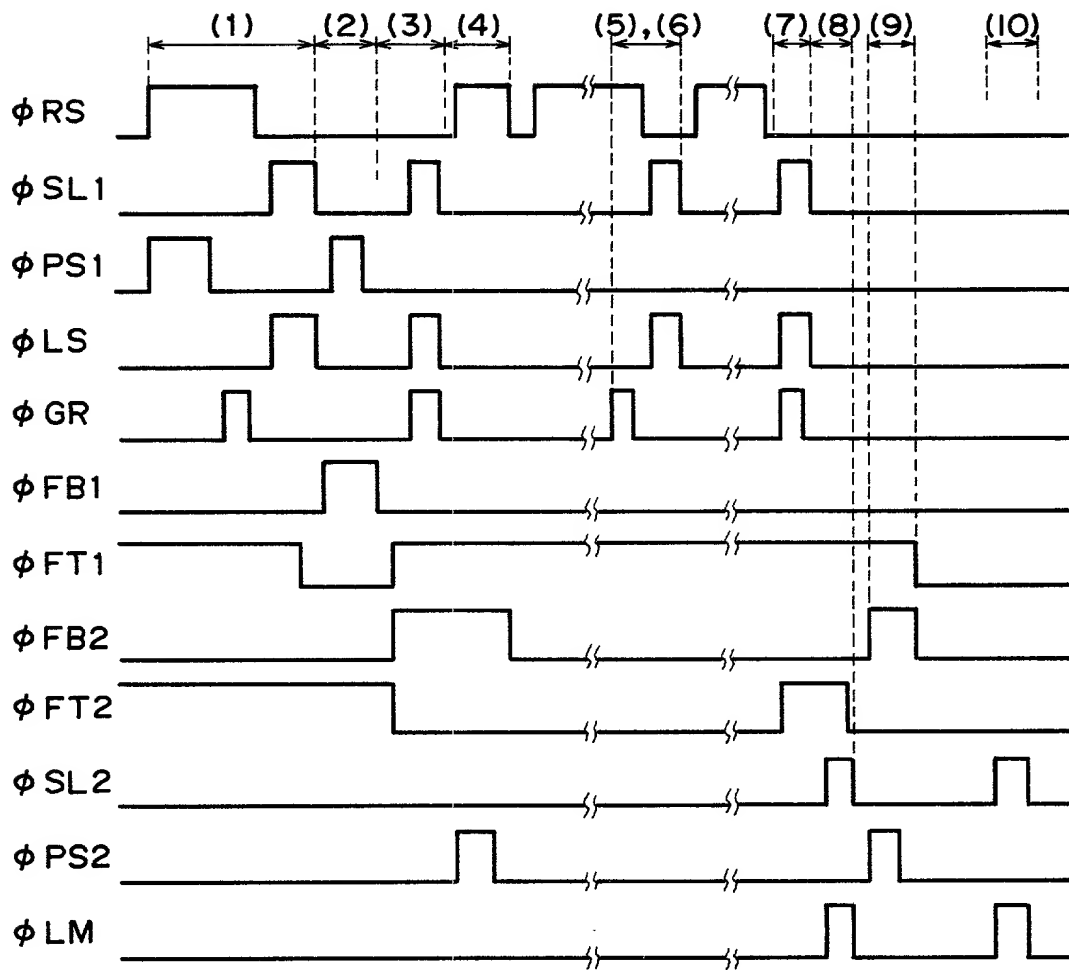


FIG. 3

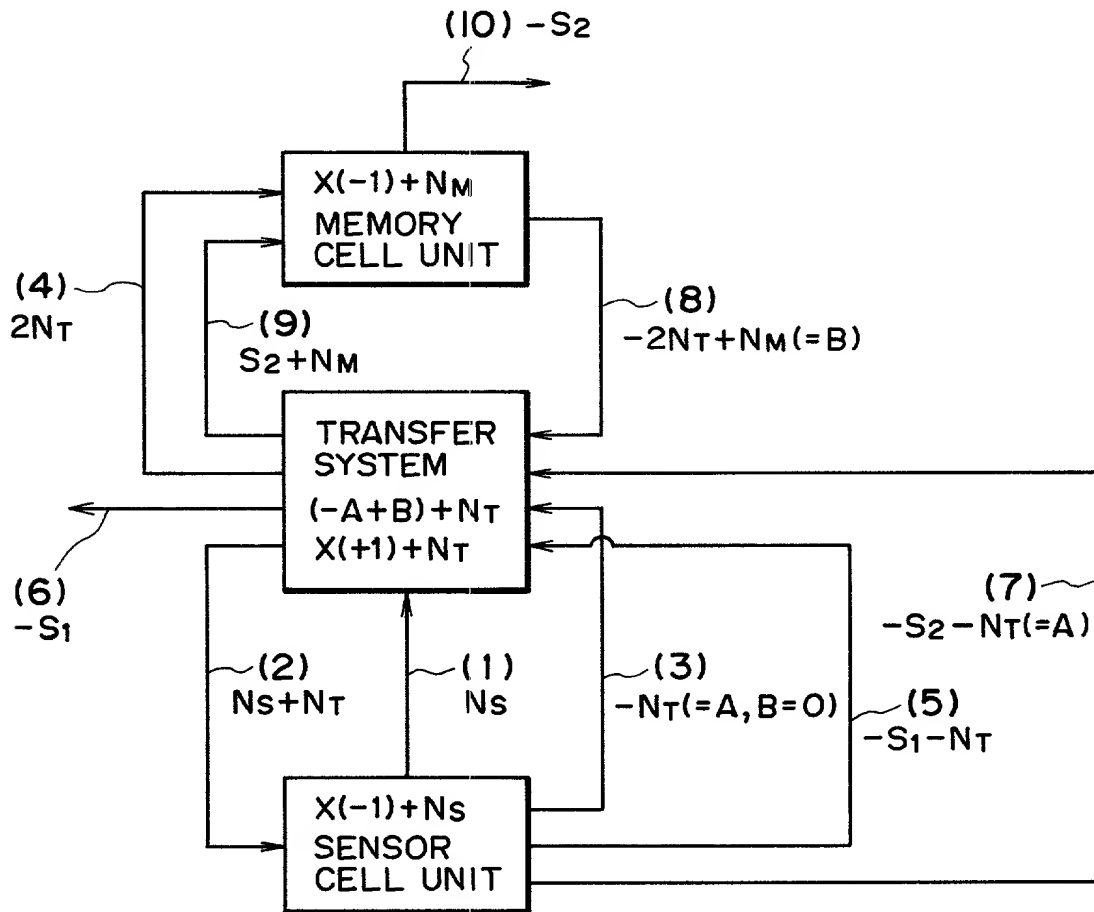


FIG. 4

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

(Page 1)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled PHOTOELECTRIC CONVERTING APPARATUS,

the specification of which ☒ is attached hereto ☐ was filed on _____ as United States Application No. or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b), of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

<u>Country</u>	<u>Application No.</u>	<u>Filed (Day/Mo./Yr.)</u>	<u>(Yes/No)</u> <u>Priority Claimed</u>
Japan	10-245216	August 31, 1998	Yes

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

<u>Application No.</u>	<u>Filed (Day/Mo./Yr.)</u>	<u>Status</u> <u>(Patented, Pending, Abandoned)</u>
------------------------	----------------------------	--

I hereby appoint the practitioners associated with the firm and Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole or First Inventor HIDEKAZU TAKAHASHI

Inventor's signature _____

Date _____ Citizen/Subject of Japan

Residence 42-2-14-614, Higashi Naruse, Isehara-shi, Kanagawa-ken,
Japan

Post Office Address c/o CANON KABUSHIKI KAISHA
30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, Japan